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Remarks

Claims 1-6 are currently pending in the patent application. For the reasons and arguments set forth below, Applicant respectfully maintains that the claimed invention is allowable over the cited references.

The Office Action dated March 13, 2007 indicated that claims 1 and 6 stand rejected under 35 U.S.C. § 103(a) over Feuerstraeter *et al.* (U.S. Publ. 2003/0058894) "AAPA" (Applicant's Admitted Prior Art) and Ishikuri (U.S. 6,674,681); claims 2 and 3 stand rejected under 35 U.S.C. § 103(a) over Feuerstraeter, AAPA, and Ishikuri as applied to claim 1, and further in view of Bongiorno *et al.* (U.S. 6,292,045); and claims 4 and 5 stand rejected under 35 U.S.C. § 103(a) over Feuerstraeter, AAPA and Ishikuri, and further in view of Werle (U.S. 5,778,002).

Applicant notes that the previous objections to Figure 1 have been overcome.

Applicant respectfully traverses the Section 103(a) rejection of claims 1-6, all of which rely upon the combination of the AAPA with the Feuerstraeter and Ishikuri references, because the cited portions of the Feuerstraeter and Ishikuri references fail to correspond to numerous claimed limitations. As acknowledged by the Examiner, the AAPA does not teach a system base chip, an interface circuit or a serial/parallel converter. The Examiner then asserts that portions of the Feuerstraeter reference teach these elements and that these portions can be combined with the AAPA's use LIN (Local Interconnect Network) protocols. However, the Examiner has failed to show how the LAN and WAN-based circuits in the cited Feuerstraeter reference could operate using a LIN protocol or otherwise correspond to the claimed limitations. The Feuerstraeter reference operates in a dual-protocol environment involving the use of both WAN and LAN protocols; LIN systems operate using only the LIN-protocol. Applicant has reviewed the Feuerstraeter reference and cannot ascertain how the proposed combination would or could correspond to the claimed limitations; no portion of the Feuerstraeter reference mentions the LIN protocol or describes any aspect of the indicated system that could operate with protocols other than WAN or LAN protocols.

In addition to the incompatibilities between Feuerstraeter's LAN and WAN devices and LIN-based systems, various other portions of Feuerstraeter cited by the Examiner do not correspond to the claimed limitations as suggested. For example, item

340 in FIG. 3 of Feuerstraeter, which is asserted by the Examiner as corresponding to the claimed system base chip is in fact a "Physical Media Attachment layer" (PMA layer) that holds serializers that respectively convert parallel data to serial data and serial data to parallel data for LAN and WAN applications. The Examiner has not shown, and the Applicant cannot ascertain, how the PMA layer 340 could function as the system base chip in a LIN-protocol environment as suggested by the Examiner.

The cited portions of the Feuerstraeter reference also do not correspond to claimed limitations directed to the system base chip having a monitoring function. The Examiner cites to item 700 in Figure 7 of Feuerstraeter as corresponding to the claimed monitoring function. However, the Examiner fails to show how the PMA layer 340 carries out monitoring functions in item 700 of Figure 7; these monitoring functions are not discussed in connection with the PMA layer 340 or with any related functions thereof (*i.e.*, the Feuerstraeter reference does not teach the claimed limitations as arranged). In the Response to Arguments section of the instant Office Action (*see, e.g.*, page 7:16-19) the Examiner alleges that item 700 of Figure 7 describes an incoming data stream detected at the input of the deserializer 360 that is shown in Figure 3 as being part of PMA layer 340. However, the Feuerstraeter reference does not teach that item 700 is referring to detecting an incoming data stream of deserializer 360. The Feuerstraeter reference teaches that a data rate detection unit 420 of deserializer 405 detects the reception of an incoming data stream and determines the rate of data transfer (*see, e.g.*, Paragraphs 0044 and 0047), which is consistent with the discussion of Figure 7 (*see, e.g.*, Paragraph 0063). Applicant submits that the deserializer referred to in connection with Figure 7 is deserializer 405, not deserializer 360 as alleged by the Examiner. Thus the Examiner has failed to show that PMA layer 340 carries out monitoring functions as does the system base chip of the claimed invention.

The cited portions of the Feuerstraeter reference also fail to correspond to claimed limitations directed to the serial/parallel converter that uses a bit-rate detected by an interface circuit in converting data. The Examiner cites to data rate detection unit 420 and to serializer 350/deserializer 360 of Feuerstraeter as corresponding to the claimed interface circuit and the serial/parallel converter respectively. However, the cited portions of the Feuerstraeter do not teach that serializer 350/deserializer 360 of PMA layer 340, which are depicted in Figure 3, make use of the data rate determined by data

rate detection unit 420, which is depicted in Figure 4. *See, e.g.,* Paragraphs 0037, 0044 and 0047. Thus, the Examiner has failed to show that the cited portions of the Feuerstraeter reference correspond to the claimed limitations.

In addition to the above lack of correspondence in the Feuerstraeter reference, the cited portions of the Ishikuri reference also do not correspond to the claimed limitations directed to the system voltage supply and the system reset. The Examiner suggests adding a power on clear (POC) circuit and a system reset (POC circuit 1) from the Ishikuri reference to the AAPA and asserts that this addition teaches the claimed system voltage supply and system reset functions. The POC circuit 1 not only fails to correspond to the claimed power supply, it cannot act as such as its function is to work independently from such a power supply. Generally, POC circuits operate independently from a system power supply, and provide functionality that is independent from the same (*see, e.g.*, the Abstract and Background of the Ishikuri reference. For example, as described at Col. 5:52-55 in Ishikuri, the POC circuit 1 includes a detection voltage source 5 that does not correspond to a system voltage supply, which is separate from the POC circuit 1 (*e.g.*, the POC circuit 1 conducts a system reset when the system power supply drops below a certain voltage level as described at Col. 5:57-60). The Examiner in the Response to Argument Section of the instant Office Action (*see, e.g.,* Page 8:2-9) appears to be confusing Ishikuri's POC circuit 1 with a circuit that receives a voltage, converts that voltage into a supply voltage and then provides the supply voltage to other components. Ishikuri's POC circuit 1 receives a power supply voltage and provides a POC output signal to AND gate 12; the POC circuit is not providing any power to the other parts of integrated circuit 100, it simply monitors the power supply voltage and provides a reset signal when the supply voltage drops below a certain level. *See, e.g.,* Figure 1 and Col. 5:43-60. Accordingly, Ishikuri's POC circuit 1 does not correspond to the claimed system voltage supply.

In view of the above, the Section 103(a) rejection of claims 1-6 is improper and Applicant requests that it be withdrawn. The cited combination of references also fails to correspond to various additional limitations in the dependent claims. However, in view of the discussion above as relevant to independent claim 1, from which claims 2-6 depend, the rejection of the dependent claims is accordingly improper (if an independent

claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988)).

Applicant further traverses the Section 103(a) rejection of claims 1-6 because there is no motivation to modify the AAPA with the cited teachings of Feuerstraeter. The Examiner's asserted motivation at page 3 of the Final Office Action, citing paragraph 0011 of the Feuerstraeter reference (to allow devices in disparate communication network types "to communicate with each other when otherwise the devices would not") is inapplicable to either the AAPA or the claimed limitations. More particularly, neither the AAPA nor the claimed limitations rely on any functionality related to enabling devices using different communications protocols to communicate with each other; in this regard, the alleged motivation is inapplicable.

Generally, the AAPA discusses the problems associated with two devices, which communicate using LIN protocol, being able to use a standard SCI/UART (Serial Communication Interface/Universal Asynchronous Receiver Transmitter) interface to communicate with each other. *See, e.g.,* Applicant's Specification, Paragraph 0003. To enable communication between these devices, the AAPA requires a specially adapted interface and a specially adapted external microcontroller that performs the bit-rate detection. *See, e.g.,* Applicant's Specification, Paragraphs 0004 and 0030. The instant application includes claimed limitations that are directed to the elimination of the need for a specially adapted external microcontroller by enabling the interface circuit to perform the bit-rate detection thereby allowing the use of any available microcontroller. *See, e.g.,* Applicant's Specification, Paragraph 0013.

In this regard, the AAPA already allows two devices to communicate with each other using LIN protocols and experiences no issues relative to this communication (*i.e.*, absent Feuerstraeter's teachings, the devices *would* communicate with each other). As such, there is no motivation to modify the AAPA based upon Feuerstraeter's teachings directed to enabling devices using different protocols to communicate with each other because the devices of the AAPA are already capable of communicating with each other. Accordingly, the Section 103(a) rejection of claims 1-6 is improper and Applicant requests that it be withdrawn.

Applicant also traverses the finality of the Final Office Action because, as consistent with M.P.E.P.§706.07(a), second actions should not be final where the

Examiner introduces a new ground of rejection that is neither necessitated by Applicant's amendment of the claims nor based on information submitted in an information disclosure statement. In this instance, the claim rejections were newly presented in the Final Office Action, relying upon AAPA as the primary reference modified by various secondary references. No claim amendments were made to necessitate this new rejection, and the cited references were not submitted in an information disclosure statement. In this regard, should any claim rejections be maintained, Applicant requests that the finality of the Final Office Action be removed and that the Applicant be afforded the opportunity to respond to any remaining rejections by way of a new Office Action.

In view of the remarks above, Applicant believes that the rejections have been overcome and that the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063.

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